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OBJECTIVE / SUMMARY

- Searching for a permanent position developing embedded software and/or designing hardware for FPGAs
- A balanced mix of FPGA design, embedded software development, and tool development
- Experience in application areas such as networking, including knowledge of many useful protocols and the proven ability to pick up new ones rapidly

EDUCATION

2/03 - 2/05 **UNIVERSITY OF MASSACHUSETTS** Amherst, MA
Master of Science in Electrical and Computer Engineering
Thesis: "Programming Model for Network Processing on an FPGA"
GPA 4.0 (out of 4.0)
Classes: Distributed Systems, Parallel Comp. Arch., Comp. Arch., more

8/95 - 5/99 **VIRGINIA TECH** Blacksburg, VA
Bachelor of Science in Computer Engineering
GPA 3.83 (out of 4.0)

EXPERIENCE

6/99 - Present **XILINX** Boulder, CO
Xilinx Research Lab

4/03 - Present *Networking*

- Defined a language and platform specific to the network-processing domain and a tool that generates hardware from the language
- Created example applications using this language:
  - An Aurora to gigabit Ethernet bridge, a remote procedure call (RPC) server, and a 16 port gigabit Ethernet IP router
- Managed the set up of a test environment –Linux workstations with gigabit Ethernet cards connected to FPGA boards via optical fiber
- Developed a System Generator for Networking tool
- Consulted on the development of Cliff, a tool that generates hardware for an FPGA from a Click description (language created at MIT)
- Created a multi-processor packet processing system

3/02 - 3/03 *System design*

- Designed and implemented a slot-based reconfigurable platform on top of the Virtex-2 Pro. A slot is an area of an FPGA with a fixed interface where different modules can be swapped in an out
- Invented a design methodology where configuration streams are embedded in a software object file, and a linker inserts the module into a slot to create a complete system

- Evaluated techniques through experiments implementing JPEG2000 using CoWare C and Handel-C
- Produced the initial implementation of a "software decelerator," where software running on the PowerPC embedded in the Virtex-2 Pro FPGA was made to look like a logic block
- Created a tool to generate assembly code and the logic/processor interface logic from a hardware state machine description

6/99 - 2/02 *Run-Time Reconfigurable computing (RTR)*

- Part of a team that developed the JBits development environment. JBits enables run-time reconfiguration by providing an API into the configuration bitstream of a Xilinx FPGA
- Developed JRoute, a router, as a layer on top of JBits
- Created applications that demonstrated advantages of RTR:
  - Smith-Waterman, CORDIC, Viterbi, Wavelet transform
- Helped develop the self-reconfiguring platform, which provides a configuration API that uses the embedded PowerPC in the Virtex-2 Pro and the internal configuration port (ICAP) to do self-reconfiguration

5/98 - 8/98 **IBM** Austin, TX

- Developed, tested, and maintained a set of Perl scripts for automated conversion of bias files for a parallel assembly language test case generator

5/97-8/97 **MCI** Rye Brooke, NY

- Developed several monitoring utilities for the network store and forward system being developed
- Responsible for major reworking of error handling
- Created several scripts to aid in the development and debugging of code

5/96 - 8/96 **MADISON DATA SYSTEMS** Hawthorne, NY

- Converted programs to fit compatibility standards for the GUI
- Designed programs to extract information for management reports

PUBLICATIONS / PATENTS

11 published papers, 3 granted patents, 18 pending patents
For a list, see website at http://www.kandeco.com/publications

SKILLS (KEYWORDS)

- Languages/APIs - JBits, VHDL, Verilog, Java, C/C++, assembly, XML, Perl, others
- Devices - Xilinx FPGAs (Virtex/Spartan), PowerPC, MicroBlaze, 68HC11, others
- Protocols/cores - Gigabit Ethernet, Aurora, SPI4.2, RPC, TCP, IP, UDP, MPLS, others
- Tools/OS – ISE, EDK, ModelSim, ChipScope, Ethereal, Linux, Windows, Solaris